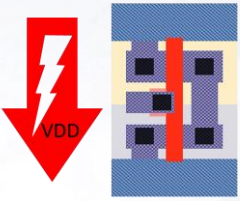
Custom-Designed
Ultralow Voltage



Digital Standard Cell Library

FYT Digital R-series Custom-Designed Digital Standard Cell Library

A collection of specialized digital standard cell intellectual property (IP) blocks used for microchip design in low to ultra-low power microchip market segment.

PROBLEM:

We recognized that there is an emerging semiconductor market segment that serves very low-power electronic devices particularly wearables, RFID tags, and IoT devices.

TARGET CUSTOMERS:

- Integrated Circuit Fabless Design House
- Researcher from Research Institutes

SOLUTION:

We are developing a unique collection of custom-designed Ultra-low Voltage Digital Cell Libraries to help chip designers from fabless design houses and system-on-chip researchers from research institutes to design microchips in this new market segment.

We believe that using our solution will **increase battery lifetime by 2X** and reduce **electricity consumption by 10X**, compared to the microchips that use the digital cell libraries currently offered in the market.

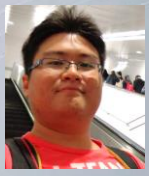
MARKET VALIDATION ACHIEVEMENT / TRACTION SALE

Currently, we are in the progress of product/ market fit validation and looking for a strategic relationship with potential clients and partners from fabless design houses, foundries and IDMs.

NEXT MILESTONE

Next, we are looking for funding from the VCs, angel investors or government agencies to facilitate us scaling up our solutions.

CEO
TARMEZEE TALIB



CTO
DR LIM YANG WEI

CSO
DR FAKHRUL ZAMAN ROKHANI

CONTACT INFO
InnoHub Putra Science Park
Universiti Putra Malaysia
Jalan Maklumat
43400 Serdang
Selangor
Malaysia

email: fzr/at/upm.edu.my

FYT DIGITAL